

WHAT IS CLAIMED IS:

5 1. A signal processing system for converting a variable frequency input signal to a fixed frequency output signal comprising:

means for generating a first clock signal at a first clock frequency;

10 means for receiving a frequency control signal that corresponds to a second frequency;

means for generating a second clock signal at the second frequency as a function of said frequency control signal;

15 means for generating a phase offset signal representing an offset in phase between the first clock signal and the second clock signal; and

means for converting a variable frequency input signal to an interpolated signal at a fixed sampling frequency in accordance with said phase offset signal.

20 2. The signal processing system of claim 1 further comprising:

means for modulating the interpolated signal onto trigonometric signals; and

25 means for converting the modulated signal to an analog signal.

30 3. The signal processing system of claim 1 wherein the means for converting a variable frequency input signal to an interpolated signal at a fixed sampling frequency in accordance with said phase offset signal comprises an interpolator that interpolates the the variable frequency input signal by a non-integer value.

35 4. The signal processing system of claim 1 wherein the means for converting a variable frequency input signal to an

5 interpolated signal at a fixed sampling frequency in accordance with said phase offset signal comprises an interpolator that interpolates the the variable frequency input signal by an integer value.

10 5. A signal processing system for converting a variable frequency input signal to an output signal having a fixed output frequency, comprising:

means for generating a clock signal at a clock frequency equal to baud rate of said variable frequency input signal as a function of a frequency control signal;

15 means for generating a phase offset signal representing an offset in phase between a recipient clock signal and the clock signal; and

means for converting a variable frequency input signal to an interpolated signal at a fixed sampling frequency in accordance with said phase offset signal.

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6. A signal processing system, comprising:

means for providing a first clock signal at a first clock frequency;

25 oscillator means, responsive to a frequency control signal and the first clock signal for providing an output clock signal at a fixed second clock frequency and a phase offset signal representing an offset in phase between the first clock signal and the second clock signal, and

30 interpolation means for offseting a pair of variable frequency input signals in accordance with the phase offset signal to provide an interpolated signal at a fixed output sampling frequency.

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5 7. The signal processing system of claim 6 wherein
the phase offset signal is greater than or equal to zero and
less than one.

10 8. The signal processing system of claim 6 wherein
the interpolation means interpolates the variable frequency
input signal by a non-integer value.

15 9. The signal processing system of claim 6 wherein
the interpolation means interpolates the variable frequency
input signal by an integer value.

20 10. The signal processing system of claim 6 further
comprising a modulator for modulating the interpolated signal
onto a trigonometric signal at a carrier frequency.

25 11. The signal processing system of claim 10 further
comprising a digital to analog converter for converting the
modulated signal to an analog signal.

30 12. The signal processing system of claim 6 wherein said
interpolation means includes a register, responsive to said
second clock signal, to provide said pair of variable
frequency input signals.